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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	:	
John U. KNICKERBOCKER, et al.	:	
Serial No.: 09/817,843	:	Art Unit: 2826
Filed: March 26, 2001	:	Examiner: L. Andujar
For: METHOD AND STRUCTURE FOR AN ORGANIC PACKAGE WITH IMPROVED BGA LIFE	:	Atty Docket: END920000008US1

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Reply Brief is filed under 37 CFR 41.41 in reply to the Examiner's Answer mailed December 3, 2004. The Applicant requests that the Appeal be maintained.

This Brief presents additional evidence in the form of U.S. Patent 4,997,516, to Adler; Rogers Corporation, *Copper Foils for High Frequency Circuit Materials*; and Merix Corporation, *Electrodeposited vs. Rolled Copper*.

The Applicant believes this "other evidence" is admissible under 37 CFR 41.33(d)(1) because: (1) the evidence overcomes all rejections on appeal; and (2) this evidence is submitted in response to arguments newly-presented in the Examiner's Answer.

INTRODUCTION: SUMMARY OF THE INVENTION

A ball grid array (BGA) package has been disclosed in U.S. Pat. No. 5,148,265, which has ball-like connection terminals over the entire packaging surface of a carrier substrate electrically connected to a semiconductor chip by gold wire bonding. In a BGA package the terminals to be connected to the packaging substrate are formed into ball-like shapes and are arrayed over substantially the entire packaging surface without deforming the leads as the case for the QFP. Therefore the pitch between the terminals become larger, thereby making surface packaging easier. Furthermore, because the connection terminals are shorter than in a QFP package, the inductance component becomes smaller and thereby the signal transmission speed becomes greater. The resulting BGA package is therefore amenable to high speed processing.1

A conventional BGA package base includes a substrate made of an electrically insulating material such as alumina ceramic and a number of connection terminals or bumps formed on the main surface of the substrate. Each connection terminal includes a solder ball bonded to a bonding pad by way of a mass of solder. The bonding pad is formed on a main surface of a substrate treated by a predetermined plating process. The mass of solder typically consists of Pb--Sn eutectic solder or a similar, low melting point solder. The solder ball, itself, is made of a relatively high melting point solder, typically containing a high percentage of lead (Pb), as for example Pb90-Sn10. The solder ball is bonded to the plated surface of the bonding pad by means of the solder mass, thereby constituting a connection terminal. In use, the wired board is mounted on a printed board having bonding pads corresponding in arrangement to those of the wired board in such a manner that their connection terminals are respectively aligned with each other, and then the respective terminals are bonded, electrically connecting the wire board to the printed board.[2]

In the prior art BGA packages, an elastic body is inserted between a semiconductor chip and terminals of a packaging substrate for relieving thermal

[1] U.S. Patent Application Publication 2002/0137256, paragraph [0004]. This Pre-Grant publication corresponds to the present application (hereinafter "pre-grant '256").
[2] Pre-grant '256, paragraph [0005].

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stress produced due to a difference in thermal expansion between the laminate package substrate and the semiconductor chip. Semiconductor devices having such structures still have problems because of the thermal mismatch. There is much in the literature about the effect of thermal stressing on BGA life. The thermal stresses, attendant to multiple power on/off cycles, literally tear the pads off the package causing loss of electrical connection and failure. The industry is trying to overcome this by increasing the pad adhesion to the substrate surface. In contradistinction to current industry practice, *the present invention solves the problem of thermal stress-induced failure by decreasing the adhesion to the laminate.*[3]

FIG. 1 illustrates a conventional fabrication technique. Substrate 100 is shown with a copper foil having a smooth surface 103 and a rough, dendritic surface 105 bonded to a dielectric 107. It is understood that dielectric 107 can be the dielectric of a single or multilayer substrate. The surface of dielectric 107 is imparted with a rough texture through lamination with the dendritic side of the external copper foil. Turning to FIG. 2 conventional subtractive circuitization is illustrated. A negative acting photoresist 209 is applied to the upper surface of copper foil 203. After development, openings 211 are formed in the resist. FIG. 3 illustrates the prior art BGA pad after etching and stripping of the resist. BGA pad 309 is shown anchored to dielectric 307 by the dendritic copper surface 305. It is understood that substantially the entire surface topography of dielectric substrate 300 is dominated by a "replica" of the dendritic surface. *The dendritic topography provides enhanced adhesion.* During thermal stressing of the laminate, such as power on/off cycling, the BGA pads remain `anchored` to the laminate surface through this dendritic structure. As the laminate surface expands and contracts with the thermal excursions the BGA pad moves with the surface. This can place excessive stress on the package. The solder ball anchors the pad to the chip. As the

[3] Pre-grant '256, paragraph [0006] (present emphasis).

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BGA pad moves with the laminate, the stress can fracture the solder connection causing failure. *Accordingly, it would be desirable to provide enhanced BGA life. The present invention achieves this goal by reducing the adhesion of the BGA pad to the laminate.*[4]

Turning now to FIG. 4, *the present invention comprises a BGA package having decreased adhesion of the BGA pad to the laminate surface.* In a first embodiment, the upper surface 401 of dielectric substrate 400 is laminated with external copper foil 407 *but in contrast with the prior art, the present invention contacts the less adhesive, shiny side 409 of the foil with the laminate surface 405.*[5]

The most egregious errors and omissions are:

1. The Examiner ignored the arguments in the Brief by failing to consider each recitation of the claims.
2. The Examiner improperly defined claim terms because the Examiner used definitions from unrelated and irrelevant arts, such as paper and silk technologies, and not definitions from a technology related to the semiconductor packaging arts as would a person of skill in the closest art to the invention.

1. The Examiner ignored the arguments in the Brief by failing to consider each recitation of the claims.

A. The rejection of Claims 1-3 and 17-21 under 35 U.S.C. § 102(e) as anticipated by Elenius (6,441,487).

Claim 1 recites:

[4] Pre-grant '256, paragraph [0007] (present emphasis).
[5] Pre-grant '256, paragraph [0021] (present emphasis).

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> An electronic package having selectively controlled contact pad - laminate surface adhesion comprising:
> a dielectric packaging substrate having a major surface;
> a conductive foil laminated to said major surface wherein said foil has at least one side having a smooth portion thereof, and wherein said smooth portion contacts said major surface of said dielectric packaging substrate.

To make a *prima facie* case for purposes of rejecting a claim, the art asserted must at least teach each recitation of the rejected claim. Throughout the course of the prosecution of this case, the Applicant has alleged that Elenius is silent as to "foil." The Examiner's Answer persists in alleging in the Elenius device, the "conductive foil is laminated with the substrate major surface."[6] However, a search of the USPTO file of the Elenius patent, using the word find utility, nowhere finds either the term "foil," or the term "laminate." Elenius nowhere teaches "laminating" or a "foil." Rather, Elenius teaches sputtering a metal layer.

> Redistribution trace 30 and solder bump pad 26 are provided as a patterned metal layer formed over the wafer passivation layer 22 and over first passivation layer 24, above the front surface of semiconductor wafer 14. This patterned metal layer is preferably formed by first blanketing the front surface of semiconductor wafer 14 with a so-called Under Bump Metallurgy (or UBM) layer. Preferably, this UBM layer is a triple-metal stack structure of Aluminum (Al), Nickel Vanadium (NiV), and Copper (Cu); alternatively, the UBM layer could be a triple-metal stack structure of Titanium (Ti), Nickel Vanadium (NiV), and Copper (Cu) or other suitable metal structure. The UBM layer can be applied over semiconductor wafer 14 by known metal sputtering techniques. Preferably, the thickness of such applied UBM layer is approximately 2 microns. The UBM layer serves several purposes; first, it adheres to the underlying surfaces. Secondly, it acts as a solder diffusion barrier for preventing molten solder from passing into the front surface of semiconductor wafer 14. The UBM layer also serves as a "wettable" layer for solderability purposes; finally, the UBM layer serves to minimize electrical contact resistance between the ductile solder ball 28 and the conductive bond pad 18. Following application of such UBM layer, it is etched in accordance with known photolithographic techniques to provide the desired patterned metal layer, thereby

[6] Examiner's answer, page 3, lines 12-13.

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providing solder bump pad 26, redistribution trace 30, as well as the electrical contact 32 to conductive bond pad 18.[7]

A rejection under § 102 requires, at a minimum, that each claim recitation must be taught by the reference asserted against the application. Where, as here, the reference fails to disclose one or more claim recitations, the Examiner has failed to make the *prima facie* case. In view of the failure to make the *prima facie* case, the Applicants respectfully request the withdrawal of the rejection.

B. The Examiner has rejected Claims 35-37 under 35 U.S.C. § 103(a) as rendered obvious by Elenius (6,441,487) in view of Gotoh (6,204,454). The present invention discloses and recites limitations that are neither disclosed, recited, nor rendered obvious by the combination of references cited under 35 U.S.C. § 103(a).

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.[8] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[9]

First, the Applicant notes that the Examiner has mischaracterized the teachings of Gotoh. The Examiner alleges that "Gotoh discloses a conductive foil having a roughness in the range of 0.3 to 0.5 microns (col. 7/lls. 9-11)."[10] The structure to which the Examiner refers is the "connecting pad disposition portion **2a**" of Gotoh.[11] However, the

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[7] U.S. 6,441,487, Col.7, lines 1-28 (present emphasis).
[8] *See* MPEP §2143.
[9] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.
[10] Examiner's Answer, page 5, lines 7-8.
[11] 6,204,454, col. 7, line 9.

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roughness values cited relate to the surface of a copper plating and do not relate to the surface of a foil. Gotoh teaches a "conductor layer **2**, conventionally, a structure formed by providing a copper plating layer **2-2** on a copper foil **2-1**."[12] Gotoh further teaches that the "connecting pad disposition portion **2a** is provided in a predetermined part on the upper surface of the above conductor layer **2**."[13] Therefore, what Gotoh teaches as the roughness of a plating layer, the Examiner has mischaracterized as the roughness of a foil.

Elenius is completely silent as to a foil. Gotoh is silent as to the surface roughness of a copper foil. The art asserted by the Examiner fails to disclose each teaching of the claimed invention. Therefore, the Examiner has failed to make the *prima facie* case.

2. The Examiner improperly defined claim terms because the Examiner used definitions from unrelated and irrelevant arts.

The present invention defined foil as having a smooth side and a dendritic side. Moreover, the present invention claimed laminating the smooth side of the foil to the substrate.

The Examiner's Answer interprets the term "smooth" as a plane surface that does not have dendrites.[14] The specification defines copper foil to be a two-sided structure having a dendritic side, that is further treated by the supplier to enhance the roughness; and having a smooth, shiny side.[15] The Examiner further alleges that "smooth" is a relative term and gives as an example that a paper sheet is smooth compared to a polish pad, but not smooth compared to silk.[16] The example demonstrates that the Examiner mischaracterizes the specification. The

[12] 6,204,454, col. 6, lines 41-43.
[13] 6,204,454, col. 6, lines 51-53.
[14] Examiner's Answer, page 6, lines 9-11 (citing specification at page 3/lines 1-7).
[15] Pre-grant '256, paragraphs [0020-0021].
[16] See Answer, page 6, lines 13-16.

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specification specifically states that two surfaces of copper foils have differing degrees of roughness and that smooth relates to the less rough surface. That different materials have different degrees of roughness is irrelevant. What is important is that a copper foil compared to itself has a rougher and a smoother side.

The art is familiar with copper foils having two sides differing in roughness.

> Copper foil is used in the making of printed circuits. Electro-deposited copper foil, the kind of foil most commonly used, is made by depositing copper on a cylinder rotating in a copper plating bath and then stripping the layer of deposited copper foil from the cylinder. The surface of the foil adjacent to and in contact with the cylinder is a replica of the cylinder surface. Since the cylinder surface is usually polished, that copper foil surface is "shiny" and is so designated, distinguishing it from the other side, the matte side, of the copper foil. The matte side is generally crystalline with micro peaks of several microns or greater in height. The surface character of the matte side is determined by the conditions of electro-deposition - bath composition, current density, temperature, thickness of deposit, addition agents and the like.[17]

Moreover, the art conventionally laminates the "matte" or "dendritic" side to improve adhesion to the substrate.

> When the copper foil is bonded or laminated to a resinous substrate such as epoxy, polyimide, phenolic and the like, which may be reinforced with glass or other fibers, good adhesion between the copper layer and the resinous substrate is important to prevent separation in subsequent procedures such as soldering, or from thermal or mechanical stress. Accordingly, the matte side of the copper foil, rather than the shiny side, is used for lamination since the surface roughness of the matte provides better adhesion. But, the matte side along usually does not have sufficient "roughness" for good adhesion and

[17] Adler, U.S. 4,997,516, col. 1, lines 9-24 (my emphasis).

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> accordingly, the matte surface is treated to improve its adhesive strength.[18]

A person of skill in an art related to the present invention is familiar with suppliers of copper foils. Such a person would know that copper foils are generally produced by one of two manufacturing processes: electrolytic deposition and cold rolling of sheets.[19]). Moreover, it is known in the art that both types of foil are treated on one side by depositing a layer of granular, dendritic copper to increase adhesion.[20] Furthermore, it is known that, depending on type of foil, the two surfaces vary in roughness from about 5 to about 8-fold.[21]

The Examiner's Answer responds: "the term 'smooth' is a relative term and not an absolute term as suggested by the applicant."[22] The original specification defined the smooth side of copper foil in a manner consistent with industry-standard practice to relate to the two sides of the foil that inherently differ in roughness because of the various treatments applied during manufacture.

The art applied by the Examiner is irrelevant. Elenius is completely silent as to foils (Elenius relates to a sputter layer). Gotoh relates to rougher and smoother portions of a single surface, not of two different surfaces. Moreover, the Gotoh relates to a plated copper surface, not to the surface of a copper foil. None of the art proposed by the Examiner relates to copper foils and none of the art teaches laminating a smooth side of a copper foil having a shiny side and a matte side.

Conclusion.

The arguments and authorities advanced in the Appeal Brief and during the prior prosecution of the present invention are hereby re-alleged and specifically incorporated by reference.

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[18] Adler, U.S. 4,997,516, col. 1, lines 46-58 (my emphasis).
[19] See Rogers Corporation, *Copper Foils for High Frequency Circuit Materials*; Merix Corporation, *Electrodeposited vs. Rolled Copper*, Submitted in the accompanying IDS.
[20] Rogers Corporation, *Copper Foils for High Frequency Circuit Materials*, "Foil Treatment."
[21] Rogers Corporation, *Copper Foils for High Frequency Circuit Materials*, Table 1.
[22] Answer, page 6, line 14.

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In view of the above arguments, and of the arguments hereby re-alleged and incorporated by reference, the Applicant respectfully requests all claims on appeal be allowed and passed to issue.

Respectfully submitted,

By_____

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